



Attorney's Docket No.: 10559/559001/P12579/Intel Corporation

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12-123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jared W. Stark IV et al. Art Unit: 2183
Serial No.: 10/055,483 Examiner: Unknown
Assignee : Intel Corporation
Filed : January 22, 2002
Title : SELECT-FREE DYNAMIC INSTRUCTION SCHEDULING

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

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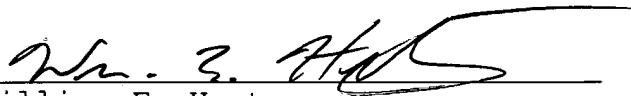
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Respectfully submitted,

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-559001	Application No. 10/055,483
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Jared W. Stark IV et al.	
		Filing Date January 22, 2002	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						

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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AC							
	AD							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AE	Ramon Canal et al., "A Low-Complexity Issue Logic", ICS 2000 Santa Fe, New Mexico, pgs. 327-335
	AF	James A. Farrell et al., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor", IEEE 1998, pgs. 707-712
	AG	Dana S. Henry et al., "Circuits for Wide-Window Superscalar Processors", ISCA 2000 Vancouver BC Canada, pgs. 236 - 247
	AH	Glenn Hinton et al., "The Microarchitecture of the Pentium® 4 Processor", Intel Technology Journal Q1, 2001, pgs. 1-13
	AI	Pierre Michaud et al., "Data-Flow Prescheduling for Large Instruction Windows in Out-of-Order Processors", IEEE 2001, pgs. 27 - 36
	AJ	Enric Moranco, et al, "Recovery Mechanism for Latency Misprediction", IEEE 2001, pgs. 118-128
	AK	Soner Önder et al., "Superscalar Execution With Dynamic Data Forwarding", Department of Computer Science, University of Pittsburgh
	AL	Subbarao Palacharla et al., "Complexity-Effective Superscalar Processors", ISCA 1997, pgs. 206-218
	AM	Jared Stark et al., "On Pipelining Dynamic Instruction Scheduling Logic", Intel Corporation, The University of Texas at Austin
	AN	Shlomo Weiss et al., "Instruction Issue Logic For Pipelined Supercomputers", IEEE 1984, pgs. 110-118
	AO	Kenneth C. Yeager, "The MIPS R10000 Superscalar Microprocessor", IEEE Micro 1996, pgs. 28-40
	AP	Michael Butler et al., "An Investigation of the Performance of Various Dynamic Scheduling Techniques", in Proceedings of the 25 th Annual ACM/IEEE International Symposium on Microarchitecture, 1992, pgs. 1-9
	AQ	Anantha Chandrakasan et al., "Design of High-Performance Microprocessor Circuits", IEEE Press, 2001
	AR	IA-32 Intel Architecture Software Developer's Manual Volume 1: Basic Architecture, Intel Corporation, 2001

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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Other Documents (include Author, Title, Date, and Place of Publication)		
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	AS	John Paul Shen, "Replenishing the Microarchitecture Treasure Chest", Carnegie-Mellon University, 1999
	AT	James E. Thornton, "Design of a Computer: The Control Data 6600", Foresman Press, 1970
	AU	R.M. Tomasulo, "An efficient algorithm for exploiting multiple arithmetic units", IBM Journal of Research and Development, Vol. 11, pgs. 25-33, January 1967

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